

REMARKS

Claims 1 and 2 have been rejected under 35 USC § 102(e) as being anticipated by Takebe '314. Applicant has canceled claims 1 and 2, rewritten claims 3 and 4 and added new claim 5. Claims 4 and 5 now contain a limitation ($n \geq 3$) which was taken from original claim 2.

In Applicant's invention as illustrated in Figure 4, Applicant shows first in Figure 4A the recordation in memory M_1 of the odd lines 011, 012, 013, 014. These are the odd lines 1 - 4 of scan 1. Next, as shown in Figure 4B, the odd line 011 is recorded in memory M_3 twice creating two odd lines 011 in two separate memories. When this occurs, the number of lines for the scan necessarily increases from 242.5 to 485 lines. Next, as shown in Figure 4C, Applicant again reads out the memory information from memory M_3 by quadruple clock and thereby generates 970 lines instead of the original 242.5 lines which are shown in Figure 4A.

In original claim 1, Applicant called for a progressive resolution circuit (29). Resolution circuit (29) is shown in greater detail in Figure 2 and includes memories M_1 and M_3 . The content of memories M_1 and M_3 is shown in Figure 4. The output of memory M_3 is shown in Figure 4C which is a non interlaced scanning signal with a higher vertical resolution than a frame signal for a TV monitor. The higher vertical resolution is clear from Figure 4C

because there are four lines representing original scan line 1 which displayed in Figure 4A.

Amended claim 4 requires reading and overlapping in the vertical direction same horizontal line data of field signals for interlace scanning. This is illustrated in Figure 4 where Applicant illustrates the same field manipulation which is of the odd field which are lines 011, 012, 013 for scan 1.

US Patent 6,356,314

'314 in the explanation of background art explains that odd numbered fields and even numbered fields are interlaced together to comprise 1 frame (1 screen) of an image which is made of odd numbered field images and even numbered field images. This is consistent with Applicant's use of the terms "odd" and "even" fields in Applicant's specification and claims.

The difference between '314 and Applicant's invention as set forth in claim 1 is stated at column 6, beginning at line 21 and continuing through line 51.

"First, the interlaced image of one field is stored in alternating address regions of the frame memory, and then the interlaced image of the other field is stored in the empty regions between the above-mentioned alternating address regions, and as a result an interlaced image is stored in the line order of the non-interlaced scan in the continuous address region of the frame memory. Therefore, reading this stored image in the address order results in the interlaced signals being converted into non-interlaced signals. Therefore, with this invention, interlaced signals can be converted into non-interlaced signals using only a single frame memory, which reduces the cost of the device and is also advantageous in terms of mounting surface area.

The eighth intervention is an image conversion method in which interlaced scan image signals composed of odd-numbered fields and even-numbered fields are converted into non-interlaced scan image signals through one frame memory, comprising: a first step of storing image signals of lines of one of the fields out of the interlaced scan image signals, corresponding to an order of the lines in the one field, in an intermittent address region in which an origin is a leading address of the frame memory emptied for each address region corresponding to one line of image data; a second step of storing image signals of lines of the other field out of the interlaced scan image signals, corresponding to an order of lines in the other field, in empty address regions formed between the intermittent address regions of the frame memory; and a third step of reading, in an address order from the leading address, the interlaced signals stored in the one frame memory."

The above description is dependent upon recording odd and even numbered fields in a single memory in alternating locations. For instance, the odd fields could be stored in memory lines 1, 3, 5, 7, . . . and the even field could be stored in memory lines 2, 4, 6, 8, When the system is to produce a non-interlaced scanning signal, the '314 device plays out the interlaced scans in the order of 1, 2, 3, 4, 5, 6, 7, Therefore, '314 utilizes both the odd and even fields when generating a non-interlaced scanning signal. It does not teach the claimed overlapping in the

vertical direction of the same horizontal line data and reading out at double speed (claim 4).

As pointed out in Applicant's specification, one purpose of Applicant's invention is to prevent blur which occurs when there is a movement between the time an odd scan occurs and an even scan occurs. This time difference is 16.7 ms as shown in Figure 5. This type of blurring will necessarily occur in '314 because both the odd and even interlace scans are used.

The Examiner has relied upon Figure 11 of '314. The description of Figure 11 begins at column 30, line 20. However, reading forward from a description of Figure 11 beginning at column 30, line 29 and continuing through column 32, line 42, it can be seen that the sub image data composed of odd numbered and even numbered fields is stored in a continuous address in the order of the non-interlaced scan lines through the above-mentioned write control for this one frame memory (20) (see column 31, lines 38 - 42). There is a high-speed clock generation circuit (12) in '314. This high-speed clock is not used for generating multiple field scans as Applicant teaches in Figures 4B and 4C. Instead, this clock is used to jump from memory location 1 to 3 to 5 to 7 for the odd line, and then provide for jumping from memory location 2 to 4 to 6 to 8 in the case of an even field. The play back, however, is not at all controlled by this high-speed clock. The description of the operation of Figure 11 is also set forth beginning in column 25, line 16 and continuing all the way through column 28, line 37. Here, the readout is described as reading the odd fields and the

even fields in sequence so that they are used in a single non-interlaced scan. In summary, the non-interlaced scan signal of '314 includes both odd and even field signals from the original output of the video device. There is no higher vertical resolution as claimed and no high density data compression in the vertical direction. Still further, there is no overlapping same field image signals as claimed.

Original Claim 2

In original claim 2 Applicant claimed non-interlaced scanning signal for one frame by reading one field signal three times or more. This is exactly the opposite of what is described in column 36, lines 48 - 63. In the '314 reference, the number of fields is reduced to one-third, not increased as Applicant claims. This limitation is now in claims 4 and 5 as ($n \geq 3$).

Amended Claim 3

In the '314 reference there is simply nothing that responds to the last paragraph of amended claim 3 which requires the read/write control circuit for reading twice a field signal in said field memory at a double speed of a write speed for the signal. Stated succinctly, '314 never doubles up the speed, but only records different field signals at different lines in a memory for a serial play out to achieve a non-interlaced scan signal.

In Applicant's claim 3, the invention requires a reading of n times the same horizontal line data of the field signal in said

field memory and further requires high-density data compression in the vertical direction. The data is then displayed on one screen thereby obtaining the non-interlaced scanning signal with higher vertical resolution than the frame signal for the TV monitor. This concept is simply not disclosed in the '314 reference.

In '314 the same data is outputted for N times in a row for the read dot clock, this same dot data (pixel data) is read and overlaps in the horizontal direction. Still further, '314 is read N times in the horizontal line data in the vertical direction. However, this is when it is enlarged to N times. Applicant's invention as set forth in claim 3 is with higher vertical resolution than the frame signal for the TV monitor. This is clearly not enlargement as taught by '314.

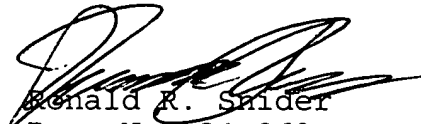
Amended Claim 4 and New Claim 5

There is simply in '314 which can respond to the last paragraph of claim 4 which requires that the signal can be read at $n (n \geq 3)$ times the speed as a write speed of the signal.

In view of the foregoing, it is respectfully submitted that the application is now in condition for allowance, and early action in accordance thereof is requested. In the event there is any reason why the application cannot be allowed in this current condition, it is respectfully requested that the Examiner contact

the undersigned at the number listed below to resolve any problems
by Interview or Examiner's Amendment.

Respectfully submitted,



Ronald R. Snider
Reg. No. 24,962

Date: December 4, 2003

Snider & Associates
Ronald R. Snider
P.O. Box 27613
Washington, D.C. 20038-7613
(202) 347-2600

RRS/bam